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10/514,421	11/16/2004	Yasuhiro Wakizawa	042978	8650

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EXAMINER	
WEDDLE, ALEXANDER MARION	
ART UNIT	PAPER NUMBER
4172	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/514,421	WAKIZAWA ET AL.	
	Examiner	Art Unit	
	ALEXANDER WEDDLE	4172	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 November 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/16/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Status of Application

1. Claims 1-5 are pending and are ready for examination on the merits.

Information Disclosure Statement

2. Those foreign patent documents listed in the information disclosure statements through which a strike-out line is drawn were not considered because the documents could not be found.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1, 2, 4, and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hosaka (JP 58-196232) in view of Mallico (US 3,892,635), Jung et al. (US 6,600,006), De Boer et al. (US 7,056,424), Zama (JP 09-186433 A), and methods, well-known at the time of the invention, for using resists and masks to form circuits in a

copper layer as taught in publications such as Rath et al. (US 6,110,643), and Appelt (US 2001/0032828).

Claim 1 claims a process of the use of a "compound capable of coordinating to a metal" which ensures pattern adhesion on a smooth insulating layer. As such, the primary reference upon which the rejection is based is Hosaka, which teaches the use of N-heterocyclic compounds for metal plating "without attacking, distorting or roughening the surface" of the insulating surface. The steps for forming an insulating layer (WO '213), "hydrophilicating" the surface (US '006), electroless plating using EDTA-Cu complex (US '424), and then creating a circuit on the copper layer with any of a variety of etching methods (*see*, for example, US '643 and US 2001/0032828) were standard steps at the time of the invention.

Claim 2 claims the process of claim 1 wherein the hydrophilicating agent is a mixture of potassium permanganate and alkali hydroxide. The claimed range for the concentration of the solution is within the range disclosed by prior art (*see*, for example, US'006).

Claim 4 claims the process of claim 2 which includes a step of heating the inner layer board after forming the conductor circuit layer.

Claim 5 claims the substrate manufactured according to the method of claim 1.

Scope and Contents of Prior Art

6. Hosaka (JP '232) teaches the use of 5-membered heterocyclic compounds, containing an N-family to provide a smooth and compact semiconductive film. Mallico (US '635) further teaches the use of 5-membered N-heterocyclic compounds in pre-

conditioning electrically insulating resin to render the substrate "suitable for metal plating without attacking distorting or roughening the surface," and that "smooth, firmly adherent electroless copper deposits are obtained on epoxy surfaces..."

Jung et al. (US '006) teaches that polymers, polyimides and norbornene specifically, can be used to form a curable insulating layer for semiconductor devices, and the Applicant admits that the curing step is standard when he states "the curing agent may be an ordinary one."

De Boer et al. (US '424), along with other publications, teaches "hydrophilicating" the surface of an insulating layer. "Permanganate solutions are utilized for etching plastics material, for example in the manufacture of printed circuit boards..." Further, "[t]hese solutions usually contain 30-100 g alkali permanganate and 30 to 100 g alkali hydroxide per 1 liter aqueous solution."

Zama (JP '433) is just one of many publications which teach electroless plating and the use of EDTA-Cu to form a conductor having uniform and high adhesive properties, and its use was known at the time of Applicant's invention.

Several methods of forming a conductor circuit on or in a thin copper layer, such as that formed by the electroless EDTA-Cu method, were known at the time of the invention. For example, Appelt (US '828) teaches the use of photoresists to form circuitry in the metal layer utilizing an etching agent comprising cupric chloride in an aqueous hydrochloric acid solution. Etching and photoresists are used to form multilayered circuit structures. Rath ('643) also teaches using cupric chloride and

hydrochloric acid to etch the metal, after which the etched circuits are stacked and pressed into a multi-layer circuit board.

Additionally, Rath('643) teaches heating the innerlayers of a circuit after forming the conductive layer by etching.

Difference between Claims and Prior Art

7. Applicant's claim 1 differs from the prior art in that it purports to combine known methods for producing a circuit to make a smoother circuit with better adhesion, where no single piece of prior art appears to combine the steps into one process. Specifically claim 1 recites combining a curable composition film containing an insulating polymer and curing agent, both of which are known in the art, with a N-heterocyclic compound, which is known to make smoother, more adhesive circuits, and using a solution of $KMnO_4$ and NaOH (or KOH) to treat the insulating layer in a known fashion, after which a known method of electroplating is carried out and a known method of etching and forming a patterned circuit is performed. Of these steps, the most significant step, according to Applicant, is the step of bringing a compound that has a structure capable of coordinating to a metal into contact with the surface of the curable composition film. According to the Applicant, his invention solves the problem of roughening the surface of the resin; "[t]o solve the problem, [the Applicant] has found that, when a layer containing a compound capable of coordinating to a metal is formed on the surface of a resin layer for solving the problem of adhesion depression, in forming wiring not roughening the surface of the resin layer, then the adhesion can be ensured."

Claim 2 recites the process of claim 1 using 65 - 150 g/liter of $KMnO_4$ and .75 - 1.5 N of alkali hydroxide. These concentrations fall exactly within the range taught by De Boer .(US '424) for the surface-treatment of electrical insulating layer. (*Cf.* De Boer, 65 g/l KMnO.sub.4 50 g/l NaOH).

Claim 4 broadly recites a step of heating the inner layer board after forming the conductive layer. This step is broad enough to read on any process which may heat the inner layer board to anneal the board, to fill voids between the inner layers, to further cure the circuitry, or to test the board for heat resistance. Rath ('643) teaches one reason for using heat after laying down the conductive layer. Other art teaches using heat for annealing the circuit (*see* Meyer et al. (US 6,221,440), which teaches annealing at 120 -150 ºC after electroless plating).

Claim 5 recites a multilayer circuit structure manufactured from the process of claim 1. Since, as explained below, claim 1 is a process which would have been obvious to one of ordinary skill in the art at the time of the invention, the multilayer circuit structure is an obvious result of the process. Furthermore, Hosaka's and Mallico's teachings show the availability and the desirability of employing N-heterocyclics to obtain a smooth insulating layer with good adhesive properties.

One of Ordinary Skill in the Art

Accordingly, the person of ordinary skill in the art is one who has knowledge of the semiconductor or electro-chemistry. Each step in the process of claim 1 is performed in the manner and in the expected order, so that performing the steps in combination would have been obvious to a person of ordinary skill in the art. Each step

of the claimed process achieves the result expected from the prior art, and the combination of steps is nothing more than a use of prior art technology in the order in which the prior art was designed to be used.

One of ordinary skill in the art would find it obvious that a an insulating layer must first be made, because the prior art teaches that step in that order; the coordinating compound must necessarily be added next as a pre-treatment to increase adhesion and smoothness, because the prior art teaches the use of such coordinating compound as a pre-treatment to increase adhesion and smoothness. To form the circuit, electroplating must occur first, and then etching or other known technique must be practiced.

In short, the motivation and teaching to combine these steps is clear from the prior art. Each step recited by Applicant's claims 1, 2, 4 achieves the same result taught by the prior art without unexpected results. Each prior art expects that the invention taught will be used in a part of the production process, forming multilayer circuits. In particular, the prior art teaches that the step given most significance by Applicant, i.e. bringing a compound capable of coordinating with a metal into contact with the surface of the film, causes the expected result: to achieve, a smooth conductive layer and better adhesion properties. The multilayer circuit of claim 5 would be desirable to make as demonstrated by Mallico and Hosaka.

Accordingly, the person of ordinary skill in the art is one who has knowledge of the semiconductor or electro-chemistry. Each step in the process of claim 1, 2, and 4 is performed in the manner and in the order expected, so that performing the steps in combination would have been obvious to a person of ordinary skill in the art. Not only

does each step bring about the expected result, but the steps occur in a logical order, as expected by the prior art.

8. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hosaka (JP '232) in view of Mallico (US '635), Jung et al. (US '006), De Boer et al. (US '424), Zama (JP '433), and methods to form circuits in a copper layer as taught in publications such as Rath et al. (US '643), and Appelt ('828) as applied to claims 1 and 2 above, and further in view of Fujifuchi et al. (JP 2000-336305) and Hashimoto (US 6,492,030).

Fujifuchi teaches coating electronic circuits with an epoxy resin with a varnish of curable resin and curing agent. The varnish used is a paint free from halogen or antimony and exhibits flame retardability, curability and moisture resistance.

Hashimoto teaches using a thermosetting polyimide resin in a method of laminating a sheet of curable insulating resin in a circuit. According to Hashimoto a metal layer can be applied to one or both sides of the laminate. In addition, Hashimoto also discloses a polyimide varnish in solvent which can be used to form the insulating layer.

Claim 3 recites a curable composition layer formed by using any method of laminating a shaped film or sheet that contains an insulating polymer and a curing agent. Clearly this reads on the prior art teaching a method of laminating a sheet containing polyimide insulating polymer and a curing agent. Moreover the recitation of a method of applying a varnish prepared by dissolving a curable composition containing an insulating polymer and a curing agent in a solvent is broad enough to read on the varnish disclosed both in Hashimoto and Fujifuchi.

Given the prior art, a person of ordinary skill in the art of semi-conductor manufacture would recognize the possibility and desirability of using both a method of lamination and a method of varnishing, the choice depending on industrial needs.

The motivation for using a varnish or lamination is to use a standard method taught in the prior art to apply the curable insulating polymer to form a semi-conductor.

Conclusion

9. No claim is allowed

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kodemura (WO 0104213), Hult (WO 2007116057), Kurosawa (EP 844283), Kaneko (JP 61041775), En et al. (US 2005/0258522), Hama (JP 2001127443), Ito et al. (JP 2000036659), Hayashi et al. (JP 2001068832), Enoki et al. (WO 0230167).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ALEXANDER WEDDLE whose telephone number is (571) 270-5346. The examiner can normally be reached on Monday-Thursday, 7:30 AM - 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vickie Kim can be reached on (571) 272-0579. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. W./
Examiner, Art Unit 4172
April 10, 2008

/Vickie Kim/
Supervisory Patent Examiner, Art Unit 4172